IN THE CLAIMS

Please amend the claims as follows:

Claims 1-15 (Canceled).

Claim 16 (New): A semiconductor memory device comprising:

a semiconductor substrate;

a first element isolating region and a second element isolating region provided in the semiconductor substrate and including a thick element isolating insulation film, for isolating an element region;

a first gate electrode provided on the element region in the semiconductor substrate in self-alignment with the first element isolation region, an upper surface of the first gate electrode being higher than the first element isolation region;

a second gate electrode having a first portion provided on the first gate electrode with the first insulation film interposed therebetween and a second portion extending on the first element isolating region, the second portion having a thickness different from that of the first portion; and

a resistance element provided on the second element isolation region, the resistance element and the second gate electrode being formed of a same material, and the resistance element and the second portion of the second gate electrode having substantially a same thickness, the resistance element not extending on the element region.

Claim 17 (New): The device according to claim 16, wherein the first gate electrode includes a first portion having a side surface in contact with a side surface of the first element isolating region.

Claim 18 (New): The device according to claim 17, wherein the first gate electrode includes a second portion projecting from an upper surface of the first element isolation region.

Claim 19 (New): The device according to claim 18, wherein the second portion of the first gate electrode has a side surface aligned with the side surface of the first portion of the first gate electrode.

Claim 20 (New): The device according to claim 16, wherein the second element isolating region includes an upper surface being higher than that of the first element isolating region.

Claim 21 (New): The device according to claim 19, wherein the second element isolating region includes an upper surface being higher than that of the first element isolating region.

Claim 22 (New): The device according to claim 16, wherein the resistance element is provided on the second element isolating region by a second insulation film formed of a same material as that of the first insulation film.

Claim 23 (New): The device according to claim 16, wherein the second portion of the second gate electrode and the resistance element are isolated from each other on the second element isolating region.

Claim 24 (New): The device according to claim 16, wherein the second element isolating region includes a part having a same height as that of the first element isolating region.

Claim 25 (New): The device according to claim 16, wherein the first gate electrode is a floating gate of a non-volatile semiconductor memory, and the second gate electrode is a control gate electrode.

Claim 26 (New): The device according to claim 16, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

Claim 27 (New): A semiconductor memory device comprising:

a semiconductor substrate;

a first element isolating insulation film and a second isolating insulation film, for isolating an element region;

a first gate electrode including a first portion having a side surface in contact with a side surface of the first element isolating insulation film and a second portion having a side surface aligned with the side surface of the first portion of the first gate

electrode, the second portion projecting from an upper surface of the first element isolating insulation film;

a second gate electrode including a first portion provided on the first gate electrode by a first insulation film and a second portion extending on the first element isolating insulation film, the second portion having a thickness different from that of the first portion; and

a resistance element provided on the second element isolating insulation film, the resistance element being formed of a same material as that of the second gate electrode, having a thickness substantially same as that of the second portion of the second gate electrode and not extending on the element region.

Claim 28 (New): The device according to claim 27, wherein the second element isolating insulation film has an upper surface higher than that of the first element isolating insulation film.

Claim 29 (New): The device according to claim 27, wherein the resistance element is provided on the second element isolating insulation film by a second insulation film formed of a same material as that of the first insulation film.

Claim 30 (New): The device according to claim 27, wherein the second portion of the second gate electrode and the resistance element are isolated from each other on the second element isolating insulation film.

Claim 31 (New): The device according to claim 27, wherein the second element isolating insulation film has a part having a same height as that of the first element isolating insulation film.

Claim 32 (New): The device according to claim 27, wherein the first gate electrode is a floating gate of a non-volatile semiconductor memory, and the second gate electrode is a control gate electrode.

Claim 33 (New): The device according to claim 27, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.